REMARKS

Claims 1-27 are all the claims pending in the application. Claims 4-5, 11-12, 19-20 and 24-25 stand rejected on informalities, and 1-27 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 4-5, 11-12, 19-20 and 24-25 stand rejected under 35 U.S.C. §112, second paragraph. The Office Action rejects the foregoing claims arguing that future or unknown technology generations cannot be claimed. In response, Applicants note that the claims do not attempt to claim a future or unknown technology. To the contrary, the claims define a system and method that provides the costs of future or unknown technologies and the two concepts are fundamentally different. Applicants agree that it would be improper to claim something that is not known. To the contrary, the claims define something that is known, that being the cost of future technology generations, the details of which are not known. Indeed, this is one of the benefits of the invention. More specifically, the invention allows the costs of future or unknown technology generations to be determined, even without the specifics of such future unknown generations being currently known.

Thus, it is Applicants position that the future or unknown technology is not currently being claimed, but instead the cost associated with future or unknown technologies is what is being claimed. This cost is well described in the specification and is free of any vagueness. Further, the claims have been amended to more clearly identify that the unknown or future technology generation is one that is "yet to be developed." Applicants submit that the revised wording, though similar in concept to the previous wording of unknown or future technologies, should be more acceptable because, while the terms of "unknown" or "future" have been proposed as being vague, the terminology "yet to be developed" more clearly describes the situation where the technology is currently unknown and will be developed in the future. In view

of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

Claims 1-7 stand rejected under 35 U.S.C. §102(b) as being anticipated by "21st Semiconductor Manufacturing Capabilities", hereinafter "Manufacturing." Claims 8-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Manufacturing in view of Evans et al., hereinafter "Evans" (6,775,647). Applicants respectfully traverse these objections/rejections based on the following discussion.

A. The Rejection Based on Manufacturing

Claims 1-7 stand rejected under 35 U.S.C. '102(b) as being anticipated by "21st Semiconductor Manufacturing Capabilities", hereinafter "Manufacturing." Applicants respectfully traverse this rejection because, for example, Manufacturing does not teach or suggest the claimed ability to "perform a regression analysis on historical costs of historical critical gate dimensions at a fabricator" to create models "only showing a relationship between said historical critical gate dimensions and said historical costs" as defined by independent claim 1. Indeed, the rejection appears to ignore that the claims are limited only to "historical critical gate dimensions" and that the models are defined as "only showing a relationship between historical critical gate dimensions and historical costs."

The April 12, 2005 preliminary amendment substantially narrowed the claims by limiting the claims to "gate dimensions." Notwithstanding this previous amendment, the rejection of independent claim 1 does not even mention how the applied reference teaches this newly added limitation. Further, the only mention of this limitation appears in the rejection of dependent claim 2 which generally points to the figures and tables of the Manufacturing reference. However, a detailed review of the Manufacturing reference finds it to be completely devoid of

any restriction regarding gate dimensions. Quite the contrary, the Figures of the Manufacturing reference compare complexity to time and cost (Figures 1 and 3); compare cost per chip elements to time (Figure 2); evaluate chip complexity, chip size, yield, etc. over time (Tables 1-5); and illustrate some models graphically (Figures 4 and 5). Nowhere does the Manufacturing reference discuss gate dimensions, much less the inventive concept of performing a regression analysis based only on historical critical gate dimensions

The Manufacturing paper is very general and describes a modeling hierarchy and establishing links and infrastructure between modeling elements to make the entire modeling environment more than the sum of individual components (see page 5, last paragraph in first column, and figure 4). In addition, the Manufacturing paper illustrates, for example, in table 5, that proper knowledge management will increase efficiency by providing knowledge to those people who need information so that they can make faster and wiser decisions (page 6, second column, last paragraph). However, other than describing these overall noble goals, the Manufacturing paper is silent regarding how such goals would be achieved. To the contrary, the claimed invention very specifically defines the ability to "perform a regression analysis on historical costs of historical critical gate dimensions" and "only showing a relationship between said historical critical gate dimensions and said historical costs". Therefore, it is Applicants' position that the Manufacturing paper does not teach or suggest any method or system that performs a regression analysis on historical costs of historical critical gate dimensions at a specific fabricator in order to create models that will allow the cost of feature designs to be simulated, as in the claimed invention.

More specifically, the Manufacturing paper describes an operational model that simulates different factory layouts. It answer questions like (quoting from page 4), "how much equipment or how many people are needed to perform a given number of activities; how can a factory be laid out for improved efficiency.." etc. Their model answers "what-if" questions concerning optimal staffing levels, tooling levels, and layout of the facility. For example, the model in the Manufacturing paper predicts the overall savings resulting from CFM vs. FFM product flow, and changes in cycle time, lot size, or operational policies. The scope of the model in the

Manufacturing paper is very broad, treating the factory floor, its area, the entity itself and the overall business enterprise as different components.

Therefore, it is Applicants' position that the Manufacturing paper does not teach or suggest the claimed ability to "perform a regression analysis on historical costs of historical critical gate dimensions at a fabricator" to create models "only showing a relationship between said historical critical gate dimensions and said historical costs" as defined by independent claim 1. Thus, Applicants submit that independent claim 1 is patentable over the Manufacturing paper. Further, dependent claims 2-7 are similarly patentable, not only because they depend from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The Rejection Based on Manufacturing and Evans

Claims 8-27 stand rejected under 35 U.S.C. '102(b) as being anticipated by "21st Semiconductor Manufacturing Capabilities", hereinafter "Manufacturing." Applicants respectfully traverse this rejection. As explained above, Manufacturing does not teach or suggest the claimed ability to "perform a regression analysis on historical costs of historical critical gate dimensions at a fabricator" to create models "only showing a relationship between said historical critical gate dimensions and said historical costs" as defined by independent claim 8 and 21 (and similarly defined by independent claim 15).

Further, Evans is referenced for teaching the ability to perform a regression analysis and is not referenced to show the ability to create models showing a relationship between historical critical gate dimensions and historical costs. Therefore, no combination of Manufacturing and Evans teaches or suggests the invention defined by independent claims 8, 15, and 21.

Applicants' first notes that Evans is non-analogous to the field of estimating semiconductor product costs as required by the preamble of the claims and as discussed in the Manufacturing reference. To the contrary, Evans relates to estimating costs within the field of

aircraft engines (column 1, lines 32-37; column 5, lines 40-50). Therefore, Applicants first notes that the Office Action fails to set forth a prima facie case of obviousness because the references are from non-analogous art fields and are not properly combinable.

Additionally, Applicants notes that even if one ordinarily skilled in the semiconductor product cost estimating field had made reference to Evans, the proposed combination of references still would not teach or suggest that the regression analysis should be limited only to historical critical gate dimensions as is required by independent claims 8, 15, and 21. As shown in the previous discussion, the Manufacturing reference does not discuss calculating future costs based upon critical gate dimensions. Instead, the Manufacturing reference only makes forecasts of chip complexity, cost per chip element set, yield percentage, etc. Evans only discusses the manufacturing of aircraft engines and is completely silent regarding any aspects of semiconductor manufacturing. Therefore, Evans also omits any teaching of limiting the regression analysis to critical gate dimensions.

Therefore, it is Applicants' position that the Manufacturing paper, even if combined with Evans, does not teach or suggest the claimed ability to "perform a regression analysis on historical costs of historical critical gate dimensions at a fabricator" to create models "only showing a relationship between said historical critical gate dimensions and said historical costs" as defined by independent claims 8 and 21 (and similarly defined by independent claim 15). Thus, Applicants submit that independent claims 8, 15, and 21 are patentable over the proposed combination of the Manufacturing paper and Evans. Further, dependent claims 9-14, 16-20, and 22-27 are similarly patentable, not only because they depend from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. Formal Matters and Conclusion

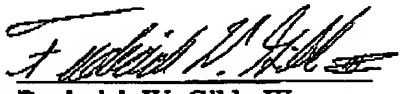
In view of the foregoing, Applicants submit that claims 1-27, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition

for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 9-20-05



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